

On the Error Effects of Random Clock Shifts in Quantum Cellular Automata Circuits

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Abstract

This paper analyzes the effect of random phase shifts in the underlying clock signals on the proper operation of several basic Quantum Cellular Automata (QCA) building blocks. Such phase shifts can result from manufacturing variations in each of the four required clock sources or from uneven path lengths. While previous literature has provided different examples of clock distribution architectures and analysis of manufacturing variations on QCA layouts, so far no literature is available on the characterization of effects resulting from the lack of phase synchronization in the QCA clocks. We perform simulations of these basic building blocks using two different simulation engines available in the QCADesigner tool. We assume that the phase shifts are characterized by a Gaussian distribution with a mean value of $i\frac{\pi}{2}$, where i is the clock number. Our results indicate that the sensitivity of building blocks to phase shifts depends on the layout of the building block, and that most building blocks were able to reliably operate under random phase shifts characterized by $\sigma = 5\%$ of $\pi/2$.

1 Introduction

The feature size of conventional field-effect transistors (FET) has been consistently decreasing in an attempt to increase device density and operating frequency of computing circuits. Today, transistors with gate lengths below 50nm are fabricated and exhibit excellent electrical characteristics [1]. This trend has resulted in an almost exponential growth in integration level of electronic chips and integrated circuits, often referred to as Moore's law [2]. The architectural and fundamental limits to this growth have been revised several times to account for new technologies but novel technological concepts (based on nano-devices and nano-electronics) are projected to play a significant role in

future systems [3] [4].

The QCA paradigm is one in which an array of cells, each interacting with its neighbors, is employed in a locally interconnected manner [5]. Research into implementing these cells using coupled quantum dots [6], nanomagnets [7], or various molecular structures [8] is ongoing. In practice, a system to clock individual cells is required for QCA operation, this involves additional wiring for clock distribution and field generation. While defect tolerance and testing of QCA circuits has been addressed in the past [9] [10], little attention has been paid to variations in the required clock network and its implications on QCA circuit operation.

We employ zone clocking in this paper, where all the cells in a design are grouped into one of four available clocking zones; each cell in a particular clocking zone is connected to one of the four available phases of the QCA clock shown in Fig. 1. Each cell in the zone is latched and unlatched synchronized with the changing clock signal.

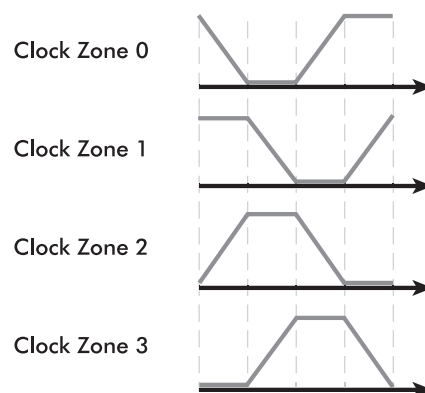


Figure 1. The four phases of the QCA clock used to control information flow in the QCA circuit.

The clock signals act to pump information throughout

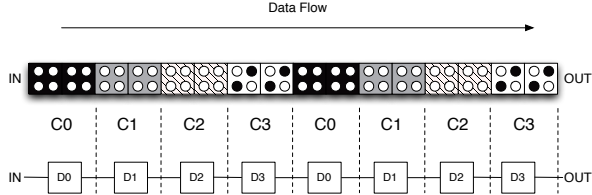


Figure 2. QCA wire shown with cells and schematic representation. C0, C1, C2, C3 are the four phases of the clock. Each of the clocking zones maps to a numbered D-latch in the circuit representation. Notice that only one clocking zone is latched.

the circuit as a result of the successive latching and unlatching in cells connected to the different clock phases. Within the zone clocking scheme, each group of cells connected to a particular phase of the clock can be considered as a D-latch [11]. As each group of cells in a particular clocking zone become latched they retain their information until the clock is relaxed, independent of changes in the polarization of neighbouring cells. A length of QCA wire can be represented schematically as shown in Fig. 2, the different clocking zones are represented with different shades of gray.

2 Contribution

In this paper, we present the results of numerical simulations of QCA building blocks in the presence of random phase variations in the individual clock signals. It is well known that process variations such as thickness, alignment, and width change occur in deep sub-micron conventional technologies. These can lead to unexpected variations in resistance, capacitance, and inductance [13], which may have adverse effects on the proper operation of such circuits. For example, it has been shown that up to 25% delay variation can be expected [14]. Clock trees and networks used for field generation and switching in QCA circuits are susceptible to such variations as well, particularly because of very fast switching and aggressive scaling of clock lines due to the inherently small size of QCA cells.

The rest of this paper is organized as follows: Section 3 presents the proposed approach to characterize different QCA building blocks in the presence of random phase shifts in the clock including a discussion of the modifications performed on QCADesigner tool to allow this study. Analysis of the various faults likely to occur due the presence of random phase shifts on the clock is discussed in Section 4. Section 5 presents the results of simulations and the robustness of various QCA building blocks followed by conclusions in

Section 6.

3 Method

In this section, we present our method of characterizing the different QCA building blocks. The goal of the simulation is to reproduce a random variation in the phase of the clock signals delivered to the different clocking zones and to evaluate its impact on the functional behavior of the building blocks.

The algorithm is summarized in Figure 3:

1. For each of the simulated layouts, we generate simulation results for the circuit without introducing any phase shifts. These results are used to automatically compare against simulations with phase shifts to determine if the circuits continue to operate properly.
2. A set of 500 batch simulations are executed using a random variable, X , to represent the possible phase shift values as a fraction of $\pi/2$. The random variable X is characterized by a Gaussian probability distribution function with mean value $\mu = i\frac{\pi}{2}$, where i is the clock number and standard deviation σ .
3. The percentage of successful circuits is recorded.
4. Step 2 is repeated for an consecutively increasing values of σ

Our objective is to obtain the success percentage as a function of σ . The chosen interval is $\sigma \in (-0.5, 0.5)$ with a step of 0.05. Therefore, phase shift values have a standard deviation $\sigma_\phi = \pi/4$ and are incremented with a step of $\pi/40$. The choice of σ_ϕ is motivated by a consideration that a higher value would increase the probability of having two clocking zones whose phases are inverted, a condition that is unlikely in reality.

3.1 Building blocks of QCA Circuits

The considered QCA building blocks are divided into wires shown in Figure 4 (Straight-wire and L-shaped Wire), logical devices shown in Figure 5 (Inverter and Majority Gate), and branches shown in Figure 6 (Fanout2 and Fanout3). The coplanar crossing is not considered in this paper.

3.2 Simulation setup

Simulations were conducted using both the bistable (time independent) and coherence vector (time dependent) simulation engines available in QCADesigner to determine if the behaviour is dependent on the particular choice of

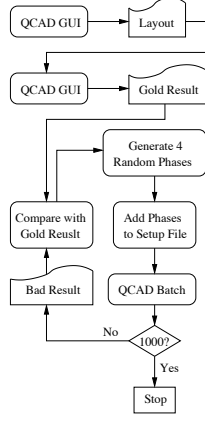


Figure 3. Flow chart of simulation procedure

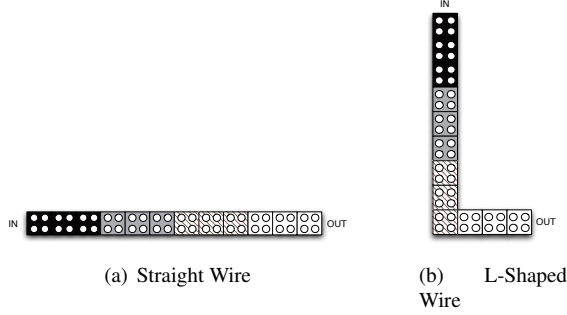


Figure 4. Simulated QCA Building blocks: (a) Straight-Wire (b) L-Shaped Wire.

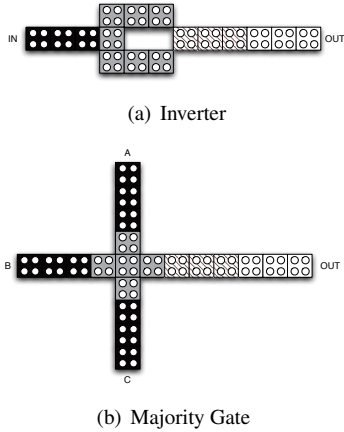
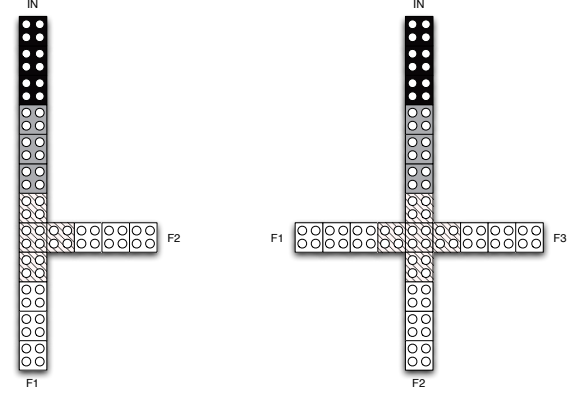


Figure 5. Simulated QCA Building blocks: (a) Inverter (b) Majority Gate.



(a) Fanout with 2 Outputs

(b) Fanout with 3 Outputs

Figure 6. Simulated QCA Building blocks: (a) Fanout 2 (b) Fanout 3.

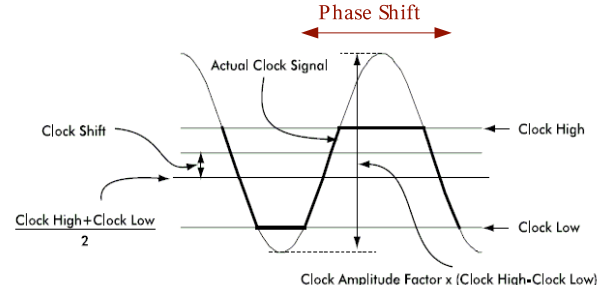


Figure 7. Phase shift on the clock waveform

selected to be 1. A set of batch simulations were run on each of the six building blocks to determine optimal values for both the Clock High and Low parameters. The relaxation time, time step, and simulation time for the coherence vector simulation engine were selected to ensure that the solver converged, while the radius of effect was chosen large enough to encapsulate the entire circuit. All other parameters were kept at their default values. A full summary of parameters used can be seen in Table 1.

The simulations required the implementation of a phase shifting capability in each of the two simulation engines within the QCADesigner tool. The clock signal in QCADesigner is calculated as a hard-saturating cosine as shown in Figure 7. The variations result in a phase shift as shown in the figure.

4 Fault Analysis

Faults due to random phase shifts in the clock can manifest themselves in one of two ways. They can result in either

model. Cell sizes of 2 nm were used throughout with ϵ_r

	Bistable Engine	Coherence Vector
Temperature	N/A	0 K
Relaxation Time	N/A	1.11 e-16 s
Time Step	N/A	1.11e-18 s
Duration	N/A	1.11 e-12 s
Clock High	7.473e-20 J	7.473e-20 J
Clock Low	1.179e-20 J	1.179e-20 J
Clock Shift	0 J	0 J
Clock Amplitude Factor	2	2
Radius of Effect	200 nm	200 nm
Relative Permittivity	1.0	1.0
Layer Separation	1.15 nm	1.15 nm
Algorithm	N/A	Euler
Randomize Cells	Yes	Yes
Animate Simulation	No	No
Number of Samples	12800	N/A
Convergence Tolerance	0.001	N/A
max Iterations per sample	100	N/A

Table 1. Simulation Parameters

an unwanted delay or inversion at the primary outputs. The delays occur because the clocking zone to which the output is connected latches out of sequence, propagating the information either sooner or later than is expected. These delays can often be masked at the output if an unwanted inversion were to occur at the same time and cause us to incorrectly identify a faulty circuit as functional. Thus, it becomes critical that the input pattern be selected appropriately such that no such false positives occur. Here, the test sequence $\{0, 0, 1, 1, 0, 1, 0, 1\}$ is selected for all QCA building blocks featuring a single input, and $\{000, 100, 110, 010, 011, 001, 101, 111\}$ for the majority gate. These test sequences ensure that the values at the primary outputs do not depend on any of its previous values.

The unwanted inversions are slightly less intuitive. Consider the fanout circuit shown in Figure 8(a). In this figure, the signal has already propagated to the cells in clocking zone C1. Here, we expect C2 to move into a latching state and propagate the signal forward. However, if phase shifts in clocking zones C2 and C3 are significant enough, then it is possible that the cells in C3 will latch before those in C2. If this occurs, then the cells in C3 will take on the opposite polarity of those in C1 due to the 45° angle that exists between their cells as shown by the NOT gates in Figure 8(b). Output F2 is not affected by this phase shift since it is lined up directly with the input and is not subject to any inversion. The same analysis can be applied to the Fanout2 building block as well.

If the Clock High value is selected appropriately ($\approx 7.473 \times 10^{-20}$ J), then there will exist some residual polariza-

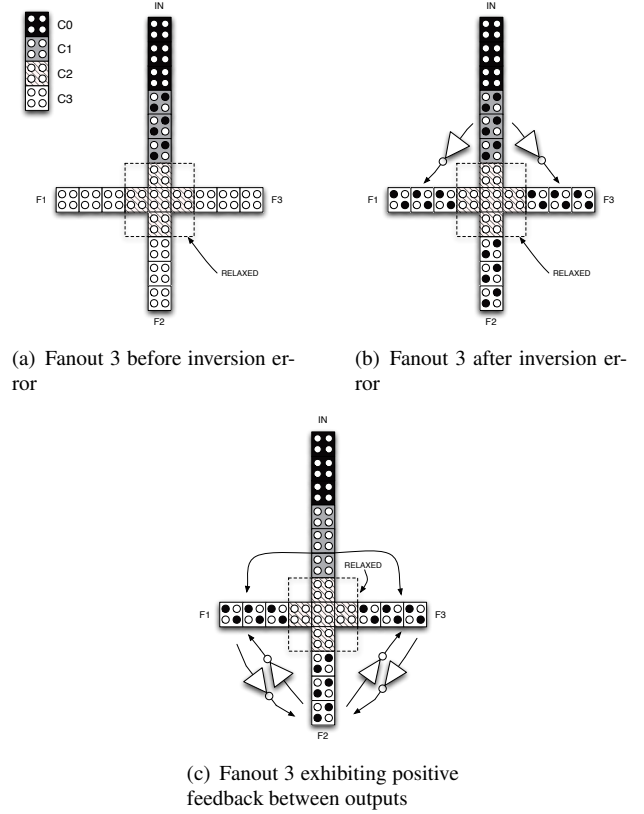


Figure 8. Inversion error in the Fanout3 circuit. If clocking zone C3 latches before C2, then two of the outputs will experience unwanted inversion (F1, F3). The different clocking zones are labelled in the top-left hand corner for reference.

tion in the cells in C2 which may be sufficient enough to perturb the cells in clocking zone C3 and overcome the inversion. However for this to occur in either of the Fanout building blocks, the residual polarization left in the cells in C2 would have to be large enough to overcome the positive feedback that occurs between the outputs as shown in Figure 8(c). Here, after output Fanout3(F2) is latched, it interacts with both Fanout3(F1) and Fanout3(F3) and helps them remain in their current state and vice-versa. Similarly, outputs Fanout3(F1) and Fanout3(F3) will interact with one another helping each other to maintain their current states. Such is not the case, however, for the L-shaped wire. The LWire building block does not have any other outputs with which to interact and therefore, may be able to recover its correct output without any corruption, providing that there exists enough residual polarization in the cells in clocking zone C2.

The majority gate behaves similarly to the Fanout3 building block. Consider the majority gate shown in Figure 9(a). Here, the signal has propagated to the cells in clocking zone C0. Assume that the variations in the clock phase have caused C2 to latch before C1. As a result, inputs A and C will have an inverting effect on the output due to the 45° angle that separates them, while input B will attempt to directly influence the output. Figures 9(b) and 9(c) outline the two possible scenarios that need to be considered under these circumstances. The first is if inputs A and C are logically opposite. If such is the case then the output will simply be equal to input B and the inverting error that occurs due to inputs A and C goes unnoticed as shown in Figure 9(b). The second scenario occurs when both inputs A and C are logically equivalent. Under these circumstances, the inverting presence of these two inputs cannot be overcome and the output will bear the incorrect result as shown in Figure 9(c).

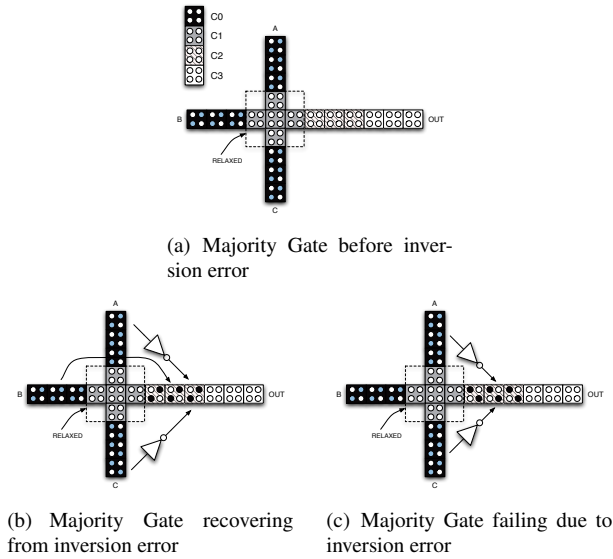


Figure 9. Inversion error in the majority gate circuit. If clocking zone C3 latches before C2, then the output may see the logical inverse of what it is supposed to. The different clocking zones are labelled in the top-left hand corner for reference.

Another example of unwanted inversion can occur in the case of the inverter. Consider Figure 10(a). Here, the cells in clocking zone C0 are holding the signal to be propagated through the inverter. If the phase shifts are such that the final clocking zone latches before C1 and C2, then the signal will propagate directly from the cells in C0 right to the output without undergoing any inversion as shown in Figure 10(b). Essentially, under this scenario, the inverter acts like a wire.

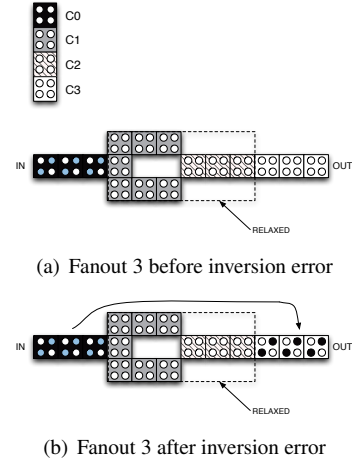


Figure 10. Inversion error in the inverter circuit. If clocking zone C3 latches before C1 and C2, then the output will simply take on the value of the input, effectively replicating the behaviour of a straight wire. The different clocking zones are labelled in the top-left hand corner for reference.

It is important to note that these circuits are simulated in a noise-less environment, *i.e.*, nothing in the circuit environment has the ability to influence a given cell other than its neighbours. All simulations are run at a temperature of 0 K in order to remove the influence of thermal noise.

5 Simulation Results

Figures 11 and 12 plot the simulation results for each of the layouts using the bistable engine and the coherence vector, respectively. For the bistable simulation engine, Figure 11 shows that circuits experiencing phase shifts in their clocking distribution network with standard deviations of up to 15% of $\pi/2$ can still operate at a 95% success rate. Similarly, from Figure 12, QCA circuits using the coherence vector simulation engine can operate at a 90% success rate while withstanding phase shifts with standard deviations of 10% of $\pi/2$ in its clocking distribution network. The non-monotonic behaviour of the results shown in Figures 11 and 12 are likely a result of relatively small number of simulations. Future work should look to expand the number of batch simulations performed.

From Figures 11 and 12, the the simulated QCA building block outputs can be grouped into one of three groups based on performance. The first group consists of outputs that resemble a straight wire, *i.e.*, represent a straight path from the input to its output. The Wire, Fanout2(F1) and

Fanout3(F2) all fall into this group of outputs. This group sees the highest success rate of any other group because the variations in clock phase can only cause delay at these outputs as mentioned in Section 4, and are not affected by any unwanted inversion.

The second group of outputs are those belonging to either Fanout2 or Fanout3 that do not see a straight path from the input to its output, i.e., there exists a 90° bend between the input and output. It is clear from Figures 11 and 12 that the outputs that belong to this group - Fanout2(F2), Fanout3(F1) and Fanout3(F2) - produce the worst success rate of any group due to the potential of unwanted inversion at the outputs as discussed in the previous section.

The third group consists of the LWire, MG, and Inverter building blocks. For reasons described in Section 4, these building blocks have success rates that lie in between the other two mentioned groups.

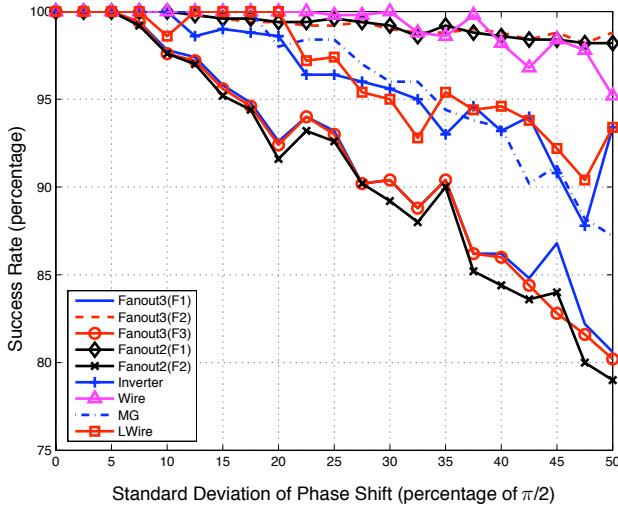


Figure 11. Success Rate vs Standard Deviation of the phase shift for the Bistable Simulation Engine.

6 Conclusion

This paper has presented an experimental evaluation of the robustness of QCA circuit building blocks against the effect of random phase shifts on the underlying clocking network. Simulations were run on a set of universal QCA building blocks, i.e., they can be used to implement arbitrary QCA circuits, and were repeated using both the bistable and coherence vector simulation engines in QCADesigner. All devices were fairly robust against variations in the clock signal phases, with success rates of

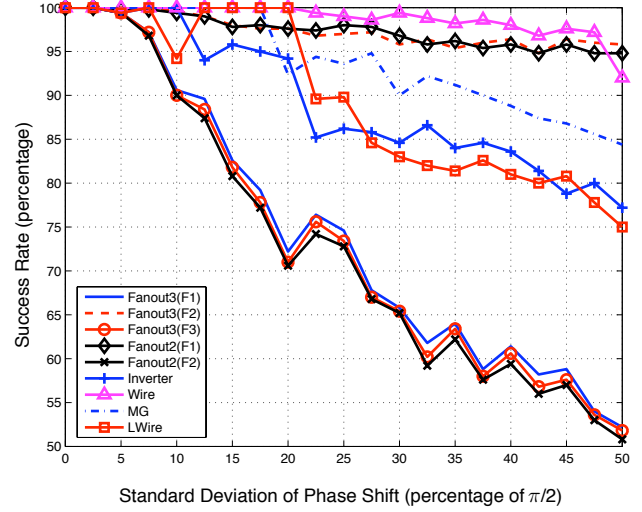


Figure 12. Success Rate vs Standard Deviation of the phase shift for the Coherence Vector Simulation Engine.

over 90% for phase shifts with standard deviations of up to 10% of $\pi/2$. We found that the success rate of a given output is highly layout-dependant. Outputs resembling a straight wire displayed more robustness to the phase variations than did those featuring kinks in their wire. As a result, QCA building blocks can be segregated into distinct classes depending on the number of kinks and outputs that they contain making it easier to pre-determine sensitive areas in a circuit due to phase variations in the clock. These results should help in developing fabrication specifications for QCA clocking networks. Additionally, the results from both simulation engines remained consistent, confirming that the behaviour of the circuits is not dependant on the choice of model.

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